### *Remarks*

In the Office Action, the Examiner noted that claims 1, 3-11, 13-18, 31-38 and 43-70 are pending in the application, and that claims 1, 3-11, 13-18, 31-38 and 43-70 are rejected. By this amendment, claims 1-30, 39-42, and 69 have been canceled, and claims 31, 34, 37, 50, 66, and 70 have been amended. Thus, claims 31-38, 43-68, and 70 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

### *In the Specification*

The Examiner required a new title that is clearly indicative of the invention to which the claims are directed. The title has been amended.

### *In the Claims*

#### Rejection Under 35 USC 112, second paragraph

The Examiner rejected claims 48-49 under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Particularly, the Examiner asserts that is it unclear how a prediction may be non-speculative. Paragraphs 96-103 of Applicant's specification describe in great detail the distinction between speculative and non-speculative predictions as the Applicant has defined them. In particular, paragraph 101 teaches that a non-speculative prediction is a prediction made with the certainty that a branch instruction exists in the current instruction stream because the branch instruction has been decoded by instruction decode logic; nevertheless, the non-speculative prediction is still a prediction because, for example, if the branch instruction is a conditional branch instruction, the branch may or may not be taken in any given execution of the branch instruction. This is in contrast to a speculative prediction, which is made without certainty that a branch instruction resides in the cache line selected by the instruction cache fetch address, which is used by the BTAC to predict the branch instruction. See paragraph 96. Because the claims are read in light of the specification,

and Applicant may be his own lexicographer, Applicant respectfully asserts that claims 48 and 49 are not indefinite, and respectfully requests the Examiner to withdraw the rejection.

## Rejection Under 35 USC 103

### 1. *Shiell* in view of *Hsu*

The Examiner rejected claims 1, 3-7, 11, 13-18, 34-38, 50-55, and 59-70 under 35 U.S.C. § 103(a) as being unpatentable over *Shiell et al.*, U.S. Patent No. 5,850,543 (hereinafter *Shiell*) in view of *Hsu et al.*, U.S. Patent No. 5,948,100 (hereinafter *Hsu*). Applicant respectfully traverses.

*Claims 34-38*

With respect to amended claim 34, Applicant respectfully asserts that claim 34 is not obviated by *Shiell* in view of *Hsu* for the reasons stated below with respect to claim 50, and respectfully requests the Examiner withdraw the rejection.

With respect to amended claim 37, Applicant respectfully asserts that *Shiell* does not teach storing a discrete indication that branching was performed if branching is performed and determining from the discrete indication, subsequent to the storing, that the branching was performed, as recited in amended claim 37. In particular, although in a remote sense storing the branch target instructions in the instruction buffer may be an indication that branching is performed, as the Examiner suggests, in any given program the instruction at the target address may be the same instruction sequentially following the branch instruction (e.g., both may be an ADD instruction); hence, it subsequently may not be possible in a given program to determine from the instructions stored in the instruction buffer whether branching was performed. For this reason, Applicant respectfully asserts that *Shiell* in view of *Hsu* does not obviate claim 37 as amended, and respectfully requests the Examiner withdraw the rejection.

Applicant respectfully asserts *Shiell* in view of *Hsu* does not obviate dependent claims 35-38 because they depend from independent claim 34, which is not obviated by *Shiell* in

view of *Hsu* for the reasons discussed above, and respectfully requests the Examiner withdraw the rejections.

*Claims 50-55, 59-65*

With respect to amended claim 50, the Examiner asserts that *Hsu* has taught a BTAC that stores an indication of whether the branch instruction presumed present in the cache line spans more than one line in the instruction cache. In particular, the Examiner asserts that *Hsu*'s cached branch instruction length is at the very least an indirect or partial indication that a branch instruction spans the cache line because it may be added to an address to determine same. Applicant respectfully asserts that *Hsu* does not teach a BTAC that stores a direct indication of whether a branch instruction presumed present in the cache line spans more than one line in the instruction cache, as recited in amended claim 50. Applicant respectfully points out that the BTAC caching and providing a direct indication may be an important distinction because it may have significant advantages, such as timing advantages. In particular, *Hsu* teaches an adder that adds the instruction length to an address to generate the span indication which requires additional propagation delay through the adder. The additional signal delay may cause the span indication signal to be the critical timing path, thereby requiring a longer microprocessor clock cycle or the addition of another pipeline stage to maintain the desired clock frequency, both of which are undesirable affects. Applicant's intention is that the discussion of the particular advantage of providing a direct indication is not intended to limit the scope of the claims beyond their ordinary meaning, and in particular is not intended to add an additional limitation into the claim regarding a particular use of the indication by the microprocessor, but rather is provided merely to illustrate to the Examiner that *Hsu*'s length plus address plus adder does not teach the direct indication of claim 50 as amended. For the reasons just stated, Applicant respectfully asserts that claim 50 as amended is not obviated by *Shiell* in view of *Hsu*, and respectfully requests the Examiner withdraw the rejection.

Applicant respectfully asserts *Shiell* in view of *Hsu* does not obviate dependent claims 51-55 and 59-65 because they depend from independent claim 50, which is not obviated

by *Shiell* in view of *Hsu* for the reasons discussed above, and respectfully requests the Examiner withdraw the rejections.

*Claims 66-68 and 70*

With respect to amended claim 66, Applicant respectfully asserts that claim 66 as amended – to incorporate the limitations of claim 69 and further amended to clarify the nature of the indication – is not obviated by *Shiell* in view of *Hsu* for the reasons stated above with respect to claim 37, and respectfully requests the Examiner withdraw the rejection.

Applicant respectfully asserts *Shiell* in view of *Hsu* does not obviate dependent claims 67-68 and 70 because they depend from independent claim 66, which is not obviated by *Shiell* in view of *Hsu* for the reasons discussed above, and respectfully requests the Examiner withdraw the rejections.

**2. *Shiell* in view of *Bae***

The Examiner rejected claims 8-10 and 56-58 under 35 U.S.C. § 103(a) as being unpatentable over *Shiell* in view of *Hsu* and further in view of *Bae et al.*, U.S. Patent No. 6,044,459 (hereinafter *Bae*). Applicant respectfully traverses.

*Claims 56-58*

Applicant respectfully asserts *Shiell* in view of *Hsu* and further in view of *Bae* does not obviate dependent claims 56-58 because they depend from independent claim 50, which is not obviated by *Shiell* in view of *Hsu* for the reasons discussed above, and respectfully requests the Examiner withdraw the rejections.

**3. *Shiell* in view of *Dietz***

The Examiner rejected claims 31-33, 43-44, and 46-49 under 35 U.S.C. § 103(a) as being unpatentable over *Shiell* in view of *Dietz et al.*, U.S. Patent No. 5,634,103 (hereinafter *Dietz*). Applicant respectfully traverses.

*Claims 31-33, 43-44 and 46-49*

With respect to amended claim 31, in the Examiner's Response to Arguments filed by Applicant on June 8, 2004, the Examiner stated that Applicant argued limitations which are not in the claim, specifically, that the indicator bit is associated with previously executed branch instructions. Applicant has amended claim 31 to clearly establish the argued limitation. Consequently, Applicant respectfully asserts that *Dietz*'s speculative bit does not indicate that a branch target address cache predicted the associated instruction is a previously executed branch instruction and that the microprocessor speculatively branched to a branch target address cached for the previously executed branch instruction, as recited in amended claim 31. Rather, *Dietz*'s speculative bit indicates whether an instruction is in a speculative execution path. Applicant cannot find an explicit definition of a "speculative execution path" in *Dietz*. However, *Dietz* clearly teaches that instructions sequentially following the branch instruction are in the speculative execution path when a branch is predicted taken and the already fetched sequential instructions are dispatched if the execution units would otherwise be idle. Col. 6, lines 4-8, 47-48. Applicant can find no other teaching in *Dietz* of which instructions are in a speculative execution path. Thus, *Dietz* impliedly teaches that the predicted branch instruction is not included in the speculative execution path, and therefore would not have its speculative bit set, if it had a speculative bit.

Furthermore, *Dietz* teaches that the fetcher, which is located before the instruction queue, removes the predicted branch instruction from the instruction stream and forwards the branch instruction to the branch prediction unit; hence, *Dietz* appears to teach that the predicted branch instruction is not even stored in *Dietz*'s instruction queue, see col. 4, lines 34-38, and therefore could not have a speculative bit associated with it even if the instruction queue were modified to include speculative bits.

Finally, *Dietz* teaches using the speculative bit to flush the sequential instructions after the predicted branch instruction, not the predicted branch instruction itself. Hence, even if *Dietz* did teach a branch instruction that had a speculative bit, based on the purpose of the speculative bit, *Dietz* does not appear to teach that the speculative bit would be set. It

is not surprising that *Dietz*'s speculative bit and the indicator of claim 31 are associated with different classes of instructions (the predicted branch instruction in claim 31; the instructions following the branch instruction in *Dietz*) since the function of the speculative bit taught by *Dietz* is different than the function of the indicator taught in at least one embodiment of Applicant's specification. In particular, Applicant's indicator is used in one embodiment for the purpose of detecting a misprediction, whereas the purpose of *Dietz*'s speculative bits is for recovering from a misprediction. In particular, as shown in the embodiment of Figure 10 and related text of Applicant's instant specification, the SB indicator is used to indicate that the associated instruction was predicted to be a branch instruction, and in particular the opcode byte of a branch instruction, so that after the instruction is decoded the prediction check logic knows to check whether the instruction is in fact a branch instruction and more specifically whether the associated byte is an opcode byte. In contrast, Applicant can find no teaching in *Dietz* in which his speculative bit is used to detect a misprediction, but rather *Dietz* teaches using the speculative bit to recover from a misprediction, namely to flush speculatively executed instructions. Applicant's intention is that the discussion of the particular embodiment is not intended to limit the scope of the claims beyond their ordinary meaning, and in particular is not intended to add an additional limitation into the claim regarding a particular use of the indicator by the microprocessor, but rather is provided merely to illustrate to the Examiner that *Dietz*'s speculative bit does not teach the indicator of claim 31.

Further with respect to amended claim 31, in the Examiner's Response to Arguments filed by Applicant on June 8, 2004, the Examiner stated that the speculative bit of *Dietz* could be stored in the instruction buffer of *Shiell* because when a branch is predicted, the instructions fetched at the predicted target address are speculative instructions and as they are fetched, they would be stored in the instruction buffer and the speculative bit may be stored with them. Even assuming *Dietz* teaches that instructions fetched at the predicted target address are included in *Dietz*'s definition of a speculative execution path and would therefore have their speculative bits set, Applicant respectfully disagrees with the Examiner in light of the amendment to claim 31 clarifying that a true value indicator is associated with the predicted branch instruction itself, i.e., not with the instructions

sequentially following the branch, as discussed above, nor with the instructions at the target address.

Because *Dietz* does not teach an instruction buffer having an indicator associated with each instruction stored therein that indicates a branch target address cache predicted the instruction is a previously executed branch instruction and that the microprocessor speculatively branched to a branch target address cached for the previously executed branch instruction, as recited in amended claim 31, Applicant respectfully asserts that claim 31 is not obviated by *Shiell* in view of *Dietz*.

With respect to claim 32, the Examiner asserts that *Dietz* teaches an instruction buffer that includes a plurality of the indicators associated with each byte of the instructions stored in the instruction buffer. Applicant respectfully disagrees. Applicant can find no teaching in *Dietz* that each byte of the instructions have an associated speculative bit. Rather, the text of *Dietz* cited by the Examiner merely teaches that each instruction has an associated speculative bit, not each byte of each instruction. This may be an important distinction since the indicator recited in claim 32 may be used to determine certain error conditions, such as whether the indicated byte is or is not an opcode byte, as described with respect to decision block 1014 of Figure 10 and related text of Applicant's instant specification. Applicant intends to make it clear that the particular embodiment just referenced is merely to illustrate to the Examiner that a distinction exists between having an indicator per byte rather than per instruction and is not intended to limit the scope of the claims beyond their ordinary meaning, and in particular is not intended to add an additional limitation into the claim regarding a particular use of the indicator by the microprocessor.

With respect to claims 43 and 44, the Examiner stated that he takes Official Notice that it is common for caches (including BTACs/BTBs) to be constructed such that multiple fetch addresses map to the same cache entry. Applicant is not aware that this is a common construction of caches, unless the Examiner is referring to multi-way associative caches in which a given index selects multiple ways in a set. However, even in the case of an associative cache, Applicant respectfully asserts that caches typically include tags

in each way that are compared with the non-index portion of the input address in order to disambiguate multiple input addresses that may index into the same entry in the cache in order to determine whether a cache hit has occurred for one unique input address in the address space. Applicant respectfully requests the Examiner to cite art in which a cache indicates a hit for multiple fetch addresses that map to the same entry. Otherwise, Applicant requests the Examiner withdraw the rejections.

Furthermore, with respect to claims 43 and 44, the Examiner has acknowledged that neither *Shiell* nor *Dietz* teaches the limitations added by claims 43 or 44, and the Examiner has not taken Official Notice that the limitations themselves are common or well-known. Instead, the Examiner has asserted that the limitations added by claims 43 and 44 would have been obvious to one of ordinary skill in the art at the time of the invention, without citing a piece of art or taking Official Notice of the added limitations. It is improper for the Examiner to combine *Shiell* with limitations the Examiner merely states as obvious but does not cite in a reference or take Official Notice of. Applicant respectfully asserts the Examiner has failed to make a *prima facie* case of obviousness and respectfully requests the Examiner withdraw the rejections.

With respect to claims 48 and 49, Applicant respectfully asserts that claims 48-49 are not obviated by *Shiell* in view of *Dietz* for reasons similar to those stated above with respect to the rejections under 35 USC 112, second paragraph, and respectfully requests the Examiner withdraw the rejection.

Applicant respectfully asserts *Shiell* in view of *Dietz* does not obviate dependent claims 32-33, 43-44, and 46-49 because they depend from independent claim 31, which is not obviated by *Shiell* and *Dietz* for the reasons discussed above.

**4. *Shiell* in view of *Dietz* further in view of *Hsu***

*Claim 45*

The Examiner rejected claim 45 under 35 U.S.C. § 103(a) as being unpatentable over *Shiell* in view of *Dietz* and further in view of *Hsu*. Applicant respectfully traverses.

The Examiner asserts that *Shiell* in view of *Dietz* has taught prediction check logic that indicates that the microprocessor erroneously branched to one of the branch target addresses if the length received from the instruction decode logic does not match a speculative length of the instruction provided by the BTAC. Applicant can find no teaching in *Shiell* or *Dietz* of prediction check logic that indicates that the microprocessor erroneously branched to one of the branch target addresses if the length received from the instruction decode logic does not match a speculative length of the instruction provided by the BTAC. Therefore, Applicant respectfully requests the Examiner withdraw the rejection.

Furthermore, Applicant respectfully asserts *Shiell* in view of *Dietz* and further in view of *Hsu* does not obviate dependent claim 45 because it depends from independent claim 31, which is not obviated by *Shiell* and *Dietz* for the reasons discussed above.

For all of the reasons advanced above, Applicant respectfully submits that claims 31-38, 43-68, and 70 are in condition for allowance. Reconsideration of the rejections is requested, and Allowance of the claims is solicited.

Applicant earnestly requests the Examiner to telephone him at the direct dial number printed below if the Examiner has any questions or suggestions concerning the application or allowance of any claims thereof.

Respectfully submitted,

E. Alan Davis

E. Alan Davis
Huffman Law Group, P.C.
Registration No. 39,954
Customer No. 23669
1832 N. Cascade Ave.
Colorado Springs, CO 80907
512.301.7234
719.623.0141 fax
alan@huffmanlaw.net

Date: 11-29-04

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By: Vicki J. Hogan